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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,738	WOLRICH ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,13,14,16-21 and 26-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 13-14,16-21,26-31,36-38,42-48* is/are rejected.

7)☒ Claim(s) *32-35 and 39-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to Amendment filed 07/10/04.

Claims 8-12, 15, 22-25 have been canceled.

Applicant's arguments filed February 06, 2002 regarding claims 1-48 have been fully considered but they are not persuasive.

Applicant argues that:

With respect to claims 1, 13, 26, 30, 36, 42:

a) Adiletta does not teach plurality of memory resources. The examiner respectfully disagrees with applicant's position. Adiletta teaches plurality of memory resources that obtain access to a push bus. Adiletta cited that "the six microengines 22a-22f access either the **SDRAM** or **SRAM**" [col. 3, lines 43-45; fig. 1, 16a, 16b]. Thus there are more than one memory resource in Adiletta's system.

b) Patkar does not disclose "memory resources obtaining access to the push bus based on arbitration by the push bus arbiter. The examiner respectfully disagrees with applicant's position. Parkar clearly teaches memory resources obtaining access to the push bus based on arbitration by the push bus arbiter. Patkar in column 3, lines 44-48 cited "note that each of the arbitrators 32-38 Push and Pull data, instructions, and/or controls signals to and from the global bus 18, with the pushing and/or pulling done in a master role (i.e., active initiation) and the other being done in a slave role (i.e., passive recipient)".

INFORMATION DISCLOSURE STATEMENT

The Applicant's submission of the IDS filed 10/07/2004 have been considered. As required by M.P.E.P. 609 C(2), copies of the PTOL-1449 is attached to the instant office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-7, 13-14, 16-19, 21, 26-28, 30-31, 34-38, 41-48 are rejected under 35 U.S.C 103(a) as being unpatentable over Adiletta PN 6,606,704, in view of Patkar et al PN 6,643,726.

Per claims 1:

Adiletta teaches a method comprising: identifying memory resources for pushing data to a processing agent; arbitrating use of a push bus by using an arbiter [Fx-cmd bus arbiter, fig. 6-1; col. 3, lines 50-60]; and pushing the data from the memory resources to the processing agent through the push bus, the memory resources obtaining access to the push bus based on arbitration by the bus arbiter [fig. 6-1, 6-2, 6-4; col. 19, lines 42-65; col. 20, lines 1-20]

Adiletta does not teach a push bus arbiter using for bus arbitration scheme.

Patkar teaches push bus arbiter [col. 3, lines 25-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the push bus arbiter into Adiletta system. By merely having a dedicate push bus arbiter for the push microengines for handling their own arbitration in a distributed manner, this dedicate arbitration scheme thus eliminates contention for memory as well as contention for a single central arbitrator. This further increase system reliability due to dual arbiter capability [e.g., push bus arbiter for push microengines, and pull bus for pull microengines] so bus arbitration can be processed over two independent data paths, enhancing speed and reliability.

Per claim 13:

Adiletta teaches the claimed limitations as mentioned above, and further teaches a system comprising; memory resources; processing agent to access the memory resources [fig. 1].

Per claim 26:

Adiletta teaches the claimed limitations as mentioned above, and further teaches a machine accessible medium, which when accessed results in a machine performing operations [fig. 1; col. 2, lines 55-67].

Per claim 30:

Adiletta teaches a method comprising: identifying memory resources for pulling data to a processing agent; arbitrating use of a pull bus by using an arbiter [Fx-cmd bus arbiter, fig.

6-1; col. 3, lines 50-60]; and pulling the data from the memory resources to the processing agent through the pull bus, the memory resources obtaining access to the pull bus based on arbitration by the bus arbiter [fig. 6-1, 6-2, 6-4; col. 19, lines 42-65; col. 20, lines 1-20]

Adiletta does not teach a pull bus arbiter using for bus arbitration scheme.

Patkar teaches pull bus arbiter [col. 3, lines 25-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include the push bus arbiter into Adiletta system. By merely having a dedicate push bus arbiter for the push microengines for handling their own arbitration in a distributed manner, this dedicate arbitration scheme thus eliminates contention for memory as well as contention for a single central arbitrator. This further increase system reliability due to dual arbiter capability [e.g., push bus arbiter for push microengines, and pull bus for pull microengines] so bus arbitration can be processed over two independent data paths, enhancing speed and reliability.

Per claim 36:

Adiletta teaches the claimed limitations as mentioned above, and further teaches a system comprising; memory resources; processing agent to access the memory resources [fig. 1].

Per claim 4:

Adiletta teaches the claimed limitations as mentioned above, and further teaches a machine accessible medium, which when accessed results in a machine performing operations [fig. 1; col. 2, lines 55-67].

Adiletta further teaches:

Per claims 2, 16 and 27:

establishing a plurality of contexts on the programming agent and maintaining program counters [col. 3, lines 20-25; col. 7, lines 35-45] and context relative registers [col. 8, lines 10-20; col. 14, lines 55-60; read/write registers (78), (80), fig. 3-2].

Per claims 3, 18 and 28:

the programming agent [16, fig. 1] executes a context and issues a read command to a memory controller in a read phase [col. 1, lines 55-60; col. 3, lines 60-67].

Per claims 4 and 19:

the memory controller processes the read command to be sent to the memory resource [col. 3, line 50 to col. 4, line 40; col. 4, lines 60-67].

Per claims 6-7, 21:

Adilleta teaches that after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer register of the programming agent; after the data has been pushed, the programming agent reads the data in the input transfer register and the programming agent continues the execution of the context [col. 3, lines 28-50; col. 8, lines 1-25; col. 19, lines 40-55].

Per claim 14:

one of the memory resources transfers data to the processing agent unidirectionally during the read phase [col. 19, lines 55-65]

Per claim 17:

the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory (DRAM) input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers [fig. 1-2].

Per claim 31:

the programming agent executes a context and loads the data into an output transfer register of the programming agent in a write phase [col. 1, lines 55-60; col. 3, lines 60-67].

Per claims 34 and 41:

the memory controller pushes the data from the output transfer register and the memory controller sends a signal to the programming agent to unlock the output transfer register [col. 19, lines 5-25].

Per claim 35:

if the context has been swapped out after the output transfer register has been unlocked, the context is swapped back in and the programming agent continues the execution of the context [col. 12, line 66 to col. 13, line 20].

Per claim 37:

the processing agent transfers data to one of the memory resources unidirectionally during the write phase [col. 19, lines 55-65].

Per claim 38:

the programming agent executes a context and loads the data into an output transfer register of the programming agent [col. 1, lines 55-60; col. 3, lines 60-67].

Per claims 43-48:

the memory resources comprises memory controller channels [26b, fig. 1; col. 3, lines 55-60].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5, 20, 29, 33, 40 are rejected under 35 U.S.C 103(a) as being unpatentable over Adiletta, and in view of Dennin et al PN 6401149.

As per claims 5, 20, 29, 33, 40:

Adilleta teaches the claimed limitations as noted above.

Adilleta does not teach the context is swapped out if the read data or if the write command is required to continue the execution of the context.

Dennin teaches a context switching process in which context or task is swapped out or in if a current read or write operation is idling for its arrival data [col. 9, lines 44-50; col. 10, lines 43-60].

It would have been obvious for one having ordinary skill in the art at the time the invention was made to swap out the lower priority context in order to execute the higher priority context because the lower priority context is idle and inactive while waiting for requested data arrival. One would be motivated to process the active context while the

other context is idle and inactive for the purpose of increasing system performance [col. 2, lines 45-60].

Allowable Subject Matter

4. **Claims 32-35, 39-41** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 (571) 272-2100 for regular communications and (703) 746-7238 for After Final communications.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

NGOC DINH
Patent Examiner
ART UNIT 2187
January 3, 2005

DONALD SPARKS
SUPERVISORY PATENT EXAMINER